REMARKS

This is in response to the Office Action mailed on September 8, 2004, and the references cited therewith. No claims have required any amendments. Reconsideration of claims 1-12 and 14-60 is respectfully solicited.

Interview Summary Not Received

The Examiner's Interview Summary of the telephonic interview between Applicant's representative, Suneel Arora, and the Examiner on June 24, 2004, was not received. Applicant requests a copy of this interview summary.

Objection to the Drawings

The drawings were objected to as not showing every feature of the invention specified in the claims. Applicant submits the attached drawing with the proposed changes show in red. In this proposed drawing, dashed lines show the first and second banks interleaved in each row in an alternating fashion as recited in claims 1-12 and 14-60.

§112 Rejection of the Claims

Claims 1-12 and 14-60 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the Office Action the Examiner stated that he did not understand the feature of "the first and second banks interleaved in each row in an alternating fashion" as recited in claims 1-12 and 14-60 and cannot see this in the drawings of the present patent application. This rejection has been carried through from the beginning of the extensive record of prosecution of the present patent application and the telephonic interview between Applicant's representative, Suneel Arora, and the Examiner on June 24, 2004, was an attempt to explain this feature to the Examiner. In the Office Action, the Examiner further stated:

IN THE DRAWINGS

Attached are proposed drawings for the Examiner with changes shown in red ink.

> Even if Fig. 3 of the present invention does show that bank 0 and bank 1 are alternately connected in each row, however, Fig. 3 and the specification do not described the different structure inside of each of banks 0 and 1. Therefore, all banks in each row in Fig. 3 are not seen to be interleaved in an alternating fashion but to be in array.

First, Applicant points out that banks 0 and 1 are not directly connected. They are connected through the sense amplifiers (346, 340, etc.). Applicant offers the following information to show how the specification defines and uses the word "bank" and "alternating."

Description / Definition of a Memory Bank

The term memory bank is well known to those skilled in the art. An explanation and definition of a memory bank can be found in Applicant's specification on page 15 through 29:

> DRDRAMs, like most commercially available memories, include memory cells that are arranged in rows and columns. Unlike many commercially available memories, however, DRDRAMs are multi-bank devices that have memory cells logically arranged into banks that can be independently accessed. This results in multiple banks within each DRDRAM, each including a number of memory cells. Gathering the memory cells into banks, and allowing different banks to undergo separate operations simultaneously, increases the overall data transfer rate of the device.
>
> Each bank is associated with one or more sense amplifiers that function to read data from, and write data to, the memory cells within the bank. The sense amplifiers serve as a data communications bridge between the banks of memory cells and the data buses external to the device. Banks are separately activated, possibly simultaneously, or overlapping in time, prior to a read or write operation. When a bank is activated, it communicates with one or more sense amplifiers. When the read or write operation is complete, the bank is deactivated, and the sense amplifiers are precharged, which readies the sense amplifiers for another operation.

Thus, a bank is a group of memory cells that are activated together. For example, all of the memory cells of Bank 0 are activated at the same time regardless if the memory cells of the bank are spread out across a wide area of the memory device. By having a second memory bank, such as Bank 1, a memory device can activate Bank 0 independent of Bank 1. The prior art shown in Figure 1 uses memory banks but does not utilize the sense amplifiers and the memory

banks in an efficient way. Applicant's invention shown in Figure 3 optimizes the use of the memory banks and sense amplifiers.

Description / Definition of Interleave and Alternate

The terms "interleave" and "alternate" are used in the specification to show how the rows of memory cells can have only two banks in each row and get better memory access with this design. The words "interleave" and "alternate" are well known to those skilled in the art and are used in the specification consistent with the normal and usual meanings. Interleave is to place one thing between another, and alternate means a choice between two choices. An explanation and definition of the words "interleave" and "alternate" can be found in Applicant's specification on page 5, lines 19 – 29:

> Figure 3 shows a multi-bank memory device in accordance with the present invention. Memory device 300 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. For example, strip 302 is a column that includes memory cells 320, 324, and 328, and strip 370 is a row that includes memory cells 320 and 330. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1).
>
> Each row in memory device 300 includes memory cores from two banks interleaved together. For example, strip 370 includes memory cores from Bank 0 and Bank 1 **alternating** across the strip. Also for example, strip 372 includes memory cores from Bank **2 interleaved** with memory cores from Bank 3.

Thus, from the foregoing, one can see that the banks in each row in Fig. 3 are interleaved in an alternating fashion between memory cells of Bank 0 and memory cells of Bank 1.

§103 Rejection of the Claims

Claims 1-12 and 14-60 were rejected under 35 USC § 103(a) as being unpatentable over Applicant's Fig. 1 designated as Prior Art. Applicant respectfully traverses this rejection in light of the arguments in support of patentability presented below.

Applicant respectfully notes that the above obviousness rejection under 35 U.S.C. § 103(a) cites only one reference to support the rejection. No second reference is combined to fulfill the elements missing from "Applicant's Fig. 1 Prior Art." Applicant therefore assumes

that the Examiner is taking Official Notice of elements in the claims (such as "interleaving") which are not found in the single reference cited. Applicant respectfully traverses this Official Notice and requests the Examiner to either 1.) cite references in support of this position pursuant to M.P.E.P. § 2144.03, or 2.) submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) to support this position.

The pending claims do not require further amendment since they already distinguish over the admitted prior art. Applicant respectfully asserts the all the claims have not been given a thorough examination and comparison to the "Applicant's Fig. 1 Prior Art" since only claim 1 is analyzed. For example, unamended claims 14, 22, 26, etc., describe interleaving between memory cores of the first and second banks. However, "Applicant's Fig. 1 Prior Art" does not show such interleaving. Further, the Examiner stated in the Office Action that "...obviously, bank 0 can be read as the first bank, bank 1 can be read as the second bank, bank 3 can be read as the first bank, bank 4 can be read as the second bank, and so on; and the memory device in Applicant's Fig. 1 Prior Art can be utilized in a computer system which includes a processor as well known in the art."

Applicant respectfully submits that the claim limitations must be given their clear meaning. Bank 0 and Bank 3 are separate elements of Applicant's claims and a proper examination cannot use the same elements of Figure 1 to read on two separate claim limitations. This is ignoring important claim limitations which distinguish over the prior art.

Since all of the elements of the claimed invention are not found in "Applicant's Fig. 1 Prior Art" cited in the First Office Action, the rejection of claims 1-12 and 14-60 under 35 U.S.C. §103(a) is incorrect. Applicant respectfully requests reconsideration of the claims and allowance of all claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10 day of January, 2005.

KACIA LEE
Name

Kacia Lee
Signature